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PATENT APPLICATION

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UNITED STATES PATENT AND TRADEMARK OFFICE

DEC 0 5 2005

Inventor(s): Christophe de Dinechin et al.

Confirmation No.: 5117

Application No.: 09/873,875

Examiner: Lillian Vo

Filing Date: June 4, 2001

Group Art Unit: 2127

Title: CONTEXT-CORRUPTING CONTEXT SWITCHING

Mail Stop
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

(X) Response/Amendment
( ) New fee as calculated below
(X) No additional fee
( ) Other: _____ (fee $_____)
( ) Petition to extend time to respond
( ) Supplemental Declaration

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	26	MINUS	26	= 0	× $50	$ 0
INDEP. CLAIMS	4	MINUS	4	= 0	× $200	$ 0
[ ] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ $360	$ 0
EXTENSION FEE	1ST MONTH $120.00 [ ]	2ND MONTH $450.00 [ ]	3RD MONTH $1020.00 [ ]	4TH MONTH $1590.00 [ ]		$ 0
					OTHER FEES	$
					TOTAL ADDITIONAL FEE FOR THIS AMENDMENT	$ 0

Charge $ 0 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

( ) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number (571) 273-8300 on 12/5/2005
Number of pages: 8

Typed Name: Hugh Gortler

Signature: _____

Respectfully submitted,

Christophe de Dinechin et al.

By _____

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- Attach as First Page to Transmitted Papers -

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In re Application of:
Christophe de Dinechin et al.
Serial No. 09/873,875
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For: **CONTEXT-CORRUPTING CONTEXT SWITCHING**

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Arlington, VA 22313-1450

SUPPLEMENTAL APPEAL BRIEF

Claims 1-26 are pending.

Claims 1-26 remain rejected.

An appeal brief was filed on June 20, 2005, but prosecution was reopened by an office action dated September 9, 2005. The office action repeats the '101 rejections of claims 1-11 and 22-26. The '101 rejections are fully addressed in the appeal brief. The following rejections are new.

'112 rejection of claim 26

The office action raises a new rejection of claim 26 under 35 USC 112, second paragraph. The office action states that claim 26 is indefinite because it isn't clear how context can be stored in both an inconsequential register and other memory.

This rejection is respectfully traversed. Claim 1 recites that the inconsequential register ***is used*** to store context. Paragraph 23 of the specification gives an example of such use: inconsequential register I is used to store the address of OS A context. The OS content can be stored at an address of the other memory.

'103 rejection of base claims 1, 12 and 22

The office action withdraws a '103 rejection of base claims 1, 12 and 22 over Bugnion et al. alone, but raises a new rejection of these claims over Bugnion et al. in view of Shaylor U.S. Patent No. 6,408,325. The new '103 rejection is respectfully traversed.

As discussed in the appeal brief, the applicant was faced with the problem of context being corrupted during a context switch. Specifically, a register is overwritten during context switching, whereby the context of that register is lost before it can be saved. This problem is specific to certain processors, such as the IA-64.

The applicant presents a solution that overcomes this problem, ***without changing the processor architecture***. Claim 1, for instance, recites a method of switching context on a processor. The method includes saving the context under software control using an inconsequential register; and preventing the processor from changing the context while the context is being saved.

According to paragraph 21 of the application, an inconsequential register is a register that is not used by the host OS at a predetermined interruption point (PIP). A point can be predetermined if the context is saved under software control (which is asynchronous) instead of hardware control (which is asynchronous). According to paragraph 22 of the application, since the context of a host OS is saved at the PIP, it is known which registers the host OS uses and which registers the host OS does not use. Therefore, the inconsequential register(s) at the PIP can be identified. The inconsequential registers can be corrupted by a virtual machine application without affecting the host OS. In particular, the context switching process can use the inconsequential registers as a temporary storage in lieu of the privileged registers.

As argued in the appeal brief, Bugnion et al. alone does not teach or suggest a solution to the problem of context corruption during context switching. Bugnion et al. does not teach or suggest the use of an inconsequential register. The examiner now appears to agree.

However, Shaylor does not teach or suggest a solution to the applicant's problem either. Shaylor addresses a different problem: during context switching, an "undesirable" number of memory operations are needed to store context from register memory to system memory (col. 2, lines 34-39).

Shaylor discusses a processor 102 that includes a plurality of registers 203. These registers 203 in the aggregate define a "context" (col. 4, lines 29-31). During a context switch, the contents of the registers 203 are stored in an area of system memory 107 (col. 4, lines 31-33). The system memory 107 is coupled to the processor 102 via a bus 101 (col. 3, lines 49-56).

Shaylor's solution is to change the processor architecture to identify only those registers 203 whose contents need to be stored or restored (col. 2, lines 57-59). Shaylor adds a "valid" bit (col. 4, lines 52-55) and a "dirty bit" (col. 4, lines 62-67) to each register 203 that stores context. The valid and dirty bits identify only those registers that need to be stored in system memory or restored from system memory Shaylor also adds an RFSA register 204 that stores the address where the context will be stored (col. 4, lines 41-44).

Shaylor does not offer a solution to the problem addressed by the applicants. Shaylor is silent about whether any of the registers 203 are corrupted during a context switch.

Shaylor proposes a change to processor architecture, whereas the applicants do not.

Shaylor's solution is performed under hardware control. Claims 1, 12 and 22 recite software control.

Shaylor does not teach or suggest using an inconsequential register to save context. Shaylor's RFSA register is not an inconsequential register. Memory 107 is system memory, not register memory.

Thus, the combined teachings of Bugnion et al. and Shaylor do not teach or suggest the method of claim 1, the apparatus of claim 12 or the software of claim 22. For these reasons alone, the '103 rejections of these base claims and their dependent claims should be withdrawn.

These rejections should be withdrawn for the additional reason that the examiner has provided no evidence whatsoever of reason, incentive, or motivation for modifying Bugnion et al. in view of Shaylor. These two documents address different problems, and offer different solutions. The examiner simply makes an unsubstantiated allegation of obviousness.

'103 rejection of base claim 11

The office action withdraws a '103 rejection of independent claim 11 over Bugnion et al. alone, but raises a new rejection of claim 11 over Bugnion et al. in view of Shaylor. The new '103 rejection is respectfully traversed.

Claim 11 recites a method of switching context between a host OS and a virtual machine on a processor. The processor has privileged registers and access to other memory. The method comprises giving the virtual machine access to the privileged registers, using at least one privileged register as temporary storage to save the context in the other memory at a predetermined interruption point, and preventing the processor from changing the context while the context is being saved. The virtual machine application controls the context switch.

The office action acknowledges that Bugnion et al. do not teach or suggest the use of privileged registers.

However, Shaylor is silent about privileged registers with respect to context switching between a host operating system and a virtual machine.

The examiner alleges that a register save area comprises privileged register memory. This is incorrect. Shaylor does not teach, hint or remotely suggest that any memory is privileged. Moreover, the register save areas 209a and 209b is not even register memory. Shaylor's Figure 2 clearly shows that the register save areas 209a and 209b are part of system memory 107.

Thus, the combined teachings of Bugnion et al. and Shaylor do not teach or suggest the method of claim 11. For this reason alone, the '103 rejection of base claim 11 should be withdrawn.

The '103 rejection of claim 11 should be withdrawn for the additional reason that the examiner has provided no evidence whatsoever of reason, incentive, or motivation for modifying Bugnion et al. in view of Shaylor. These two documents address different problems, and offer different solutions. The examiner simply makes an unsubstantiated allegation of obviousness.

For the reasons set forth in the appeal brief and this supplement brief, all claims are believed to be statutory and allowable over the documents made of record. Therefore, reinstatement of the appeal is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on December 5, 2005.

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